	L #	Hits	Search Text	DBs
1	L1	571	steer$3 near10 instruction	USPAT; US-PGPUB
2	L3	334	steer$3 near10 instruction	EPO; JPO; DERWENT; IBM_TDB
3	L4	0	3 near20 cache	EPO; JPO; DERWENT; IBM_TDB
4	L2	31	1 near20 cache	USPAT; US-PGPUB
5	L6	0	(pre-steer$3 presteer$3) near10 instruction	USPAT; US-PGPUB
6	L7	0	(pre-steer$3 presteer$3) near10 cache	USPAT; US-PGPUB
7	L9	10	((instruction adj2 (queue buffer)) reservation) near50 (steer$3 crossbar cross-bar (cross adj2 bar))	EPO; JPO; DERWENT; IBM_TDB
8	L8	97	((instruction adj2 (queue buffer)) reservation) near50 (steer$3 crossbar cross-bar (cross adj2 bar))	USPAT; US-PGPUB

	Document ID	U	Title	Current OR
1	JP 10069 389 A	☐	DEVICE THAT MAKE GOOD USE OF BRANCH PREDICTIVE CACHE WITHOUT TAG BY REARRANGEMENT OF BRANCH	
2	US 57218 93 A	☐	Non-tagged branch prediction cache exploiting for compiler - inspecting each bucket, and for buckets containing branch instructions, whose predicted directions conflict, moving one or more of conflicting branch instructions to another bucket	
3	US 55772 26 A	☐	Coherent caching I/O device for network - includes remote messages which communicate with all computers in data structure to invalidate data blocks which have addresses which correspond to those which have been written to	

	Document ID	U	Title	Current OR
1	US 20020 18882 9 A1	☐	System and method for handling load and/or store operations in a superscalar microprocessor	712/218
2	US 20020 09540 3 A1	☒	Methods to perform disk writes in a distributed shared disk system needing consistency across failures	707/1
3	US 20020 02932 8 A1	☒	High-performance, superscalar-based computer system with out-of-order instruction execution	712/23
4	US 20020 01690 3 A1	☒	High-performance, superscalar-based computer system with out-of-order instruction execution and concurrent results distribution	712/23
5	US 64346 93 B1	☒	System and method for handling load and/or store operations in a superscalar microprocessor	712/245
6	US 62826 30 B1	☒	High-performance, superscalar-based computer system with out-of-order instruction execution and concurrent results distribution	712/23
7	US 62726 19 B1	☒	High-performance, superscalar-based computer system with out-of-order instruction execution	712/41
8	US 62567 20 B1	☒	High performance, superscalar-based computer system with out-of-order instruction execution	712/23
9	US 62302 54 B1	☒	System and method for handling load and/or store operators in a superscalar microprocessor	712/23
10	US 61287 23 A	☒	High-performance, superscalar-based computer system with out-of-order instruction execution	712/23
11	US 61015 94 A	☒	High-performance, superscalar-based computer system with out-of-order instruction execution	712/41
12	US 60921 81 A	☒	High-performance, superscalar-based computer system with out-of-order instruction execution	712/206
13	US 60526 97 A	☒	Reorganization of collisions in a hash bucket of a hash table to improve system performance	707/205
14	US 60386 54 A	☒	High performance, superscalar-based computer system with out-of-order instruction execution	712/23
15	US 60386 53 A	☒	High-performance superscalar-based computer system with out-of-order instruction execution and concurrent results distribution	712/23
16	US 59875 93 A	☒	System and method for handling load and/or store operations in a superscalar microprocessor	712/206
17	US 59616 29 A	☒	High performance, superscalar-based computer system with out-of-order instruction execution	712/23
18	US 58322 92 A	☒	High-performance superscalar-based computer system with out-of-order instruction execution and concurrent results distribution	712/23
19	US 57908 22 A	☒	Method and apparatus for providing a re-ordered instruction cache in a pipelined microprocessor	712/204
20	US 57218 93 A	☒	Exploiting untagged branch prediction cache by relocating branches	712/239
21	US 56897 20 A	☒	High-performance superscalar-based computer system with out-of-order instruction execution	712/23

	Document ID	U	Title	Current OR
22	US 5659782 A	☒	System and method for handling load and/or store operations in a superscalar microprocessor	712/23
23	US 5577226 A	☒	Method and system for coherently caching I/O devices across a network	711/119
24	US 5560032 A	☒	High-performance, superscalar-based computer system with out-of-order instruction execution and concurrent results distribution	712/23
25	US 5557763 A	☒	System for handling load and/or store operations in a superscalar microprocessor	712/23
26	US 5539911 A	☒	High-performance, superscalar-based computer system with out-of-order instruction execution	712/23
27	US 5481685 A	☒	RISC microprocessor architecture implementing fast trap and exception state	712/244
28	US 5448705 A	☒	RISC microprocessor architecture implementing fast trap and exception state	712/244

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5	L6	0	(pre-steer$3 presteer$3) near10 instruction	USPAT; US-PGPUB
6	L7	0	(pre-steer$3 presteer$3) near10 cache	USPAT; US-PGPUB
7	L9	10	((instruction adj2 (queue buffer)) reservation) near50 (steer$3 crossbar cross-bar (cross adj2 bar))	EPO; JPO; DERWENT; IBM_TDB
8	L8	97	((instruction adj2 (queue buffer)) reservation) near50 (steer$3 crossbar cross-bar (cross adj2 bar))	USPAT; US-PGPUB
9	L11	3	(bin bucket) near10 cache near20 instruction	EPO; JPO; DERWENT; IBM_TDB
10	L10	28	(bin bucket) near10 cache near20 instruction	USPAT; US-PGPUB

	Document ID	U	Title	Current OR
1	US 20030023835 A1	☐	Method and system to perform a thread switching operation within a multithreaded processor based on dispatch of a quantity of instruction information for a full instruction	712/214
2	US 20030023834 A1	☒	Method and system to insert a flow marker into an instruction stream to indicate a thread switching operation within a multithreaded processor	712/214
3	US 20030023659 A1	☒	Method and apparatus for thread switching within a multithreaded processor	709/102
4	US 20030023658 A1	☒	Method and system to perform a thread switching operation within a multithreaded processor based on detection of the absence of a flow of instruction information for a thread	709/102
5	US 20030018687 A1	☒	Method and system to perform a thread switching operation within a multithreaded processor based on detection of a flow marker within an instruction information	709/102
6	US 20030018686 A1	☒	Method and system to perform a thread switching operation within a multithreaded processor based on detection of a stall condition	709/102
7	US 20030018685 A1	☒	Method and system to perform a thread switching operation within a multithreaded processor based on detection of a branch instruction	709/102
8	US 20020116600 A1	☒	Method and apparatus for processing events in a multithreaded processor	712/218
9	US 20020095614 A1	☒	Method and apparatus for disabling a clock signal within a multithreaded processor	713/500
10	US 6496925 B1	☒	Method and apparatus for processing an event occurrence within a multithreaded processor	712/244
11	US 6393549 B1	☒	Instruction alignment unit for routing variable byte-length instructions	712/204
12	US 6357016 B1	☒	Method and apparatus for disabling a clock signal within a multithreaded processor	713/601
13	US 6351804 B1	☒	Control bit vector storage for a microprocessor	712/217
14	US 6269436 B1	☒	Superscalar microprocessor configured to predict return addresses from a return stack storage	712/23
15	US 6240458 B1	☒	System and method for programmably controlling data transfer request rates between data sources and destinations in a data processing system	709/232
16	US 6189068 B1	☒	Superscalar microprocessor employing a data cache capable of performing store accesses in a single clock cycle	711/3
17	US 6157994 A	☒	Microprocessor employing and method of using a control bit vector storage for instruction execution	712/23
18	US 6131155 A	☒	Programmer-visible uncached load/store unit having burst capability	712/207
19	US 6115359 A	☒	Elastic bandwidth explicit rate (ER) ABR flow control for ATM switches	370/232
20	US 6091709 A	☒	Quality of service management for packet switched networks	370/235

	Document ID	U	Title	Current OR
21	US 6081656 A	☒	Method for deriving a double frequency microprocessor from an existing microprocessor	716/3
22	US 6079006 A	☒	Stride-based data address prediction structure	711/213
23	US 6065110 A	☒	Method and apparatus for loading an instruction buffer of a processor capable of out-of-order instruction issue	712/217
24	US 6014734 A	☒	Superscalar microprocessor configured to predict return addresses from a return stack storage	712/23
25	US 6006324 A	☒	High performance superscalar alignment unit	712/204
26	US 5987587 A	☒	Single chip multiprocessor with shared execution units	712/23
27	US 5987561 A	☒	Superscalar microprocessor employing a data cache capable of performing store accesses in a single clock cycle	711/3
28	US 5983336 A	☒	Method and apparatus for packing and unpacking wide instruction word using pointers and masks to shift word syllables to designated execution units groups	712/24
29	US 5978907 A	☒	Delayed update register for an array	712/239
30	US 5978899 A	☒	Apparatus and method for parallel processing and self-timed serial marking of variable length instructions	712/210
31	US 5968169 A	☒	Superscalar microprocessor stack structure for judging validity of predicted subroutine return addresses	712/239
32	US 5958048 A	☒	Architectural support for software pipelining of nested loops	712/241
33	US 5958041 A	☒	Latency prediction in a pipelined microarchitecture	712/214
34	US 5949789 A	☒	Arbitration ring for accessing a limited bandwidth switching network	370/452
35	US 5935239 A	☒	Parallel mask decoder and method for generating said mask	712/224
36	US 5933618 A	☒	Speculative register storage for storing speculative results corresponding to register updated by a plurality of concurrently recorded instruction	712/217
37	US 5928355 A	☒	Apparatus for reducing instruction issue stage stalls through use of a staging register	712/214
38	US 5923871 A	☒	Multifunctional execution unit having independently operable adder and multiplier	712/221
39	US 5918034 A	☒	Method for decoupling pipeline stages	712/218
40	US 5912889 A	☒	ATM switch with output port clustering for dynamically allocating bandwidth between ports	370/359
41	US 5909587 A	☒	Multi-chip superscalar microprocessor module	712/1
42	US 5898852 A	☒	Load instruction steering in a dual data cache microarchitecture	712/214
43	US 5892936 A	☒	Speculative register file for storing speculative register states and removing dependencies between instructions utilizing the register	712/216

	Document ID	U	Title	Current OR
44	US 5889985 A	☒	Array prefetch apparatus and method	712/225
45	US 5887152 A	☒	Load/store unit with multiple oldest outstanding instruction pointers for completing store and load/store miss instructions	712/217
46	US 5883895 A	☒	Arbitration ring with automatic sizing for a partially populated switching network	370/462
47	US 5881279 A	☒	Method and apparatus for handling invalid opcode faults via execution of an event-signaling micro-operation	712/244
48	US 5881278 A	☒	Return address prediction system which adjusts the contents of return stack storage to enable continued prediction after a mispredicted branch	712/242
49	US 5878255 A	☒	Update unit for providing a delayed update to a branch prediction array	712/240
50	US 5875324 A	☒	Superscalar microprocessor which delays update of branch prediction information in response to branch misprediction until a subsequent idle clock	712/238
51	US 5875315 A	☒	Parallel and scalable instruction scanning unit	712/204
52	US 5867701 A	☒	System for inserting a supplemental micro-operation flow into a macroinstruction-generated micro-operation flow	712/248
53	US 5864707 A	☒	Superscalar microprocessor configured to predict return addresses from a return stack storage	712/23
54	US 5860104 A	☒	Data cache which speculatively updates a predicted data cache storage location with store data and subsequently corrects mispredicted updates	711/137
55	US 5859991 A	☒	Parallel and scalable method for identifying valid instructions and a superscalar microprocessor including an instruction scanning unit employing the method	712/204
56	US 5854921 A	☒	Stride-based data address prediction structure	712/239
57	US 5848433 A	☒	Way prediction unit and a method for operating the same	711/137
58	US 5845100 A	☒	Dual instruction buffers with a bypass bus and rotator for a decoder of multiple instructions of variable length	712/204
59	US 5835491 A	☒	Method for supporting multicast capabilities in switching networks with a reservation ring	370/386
60	US 5832297 A	☒	Superscalar microprocessor load/store unit employing a unified buffer and separate pointers for load and store operations	710/5
61	US 5832249 A	☒	High performance superscalar alignment unit	712/204
62	US 5826071 A	☒	Parallel mask decoder and method for generating said mask	712/224
63	US 5822574 A	☒	Functional unit with a pointer for mispredicted resolution, and a superscalar microprocessor employing the same	712/233
64	US 5822560 A	☒	Apparatus for efficient instruction execution via variable issue and variable control vectors per issue	712/214
65	US 5822559 A	☒	Apparatus and method for aligning variable byte-length instructions to a plurality of issue positions	712/214
66	US 5822558 A	☒	Method and apparatus for predecoding variable byte-length instructions within a superscalar microprocessor	712/213

	Document ID	U	Title	Current OR
67	US 58225 55 A	☒	Method and apparatus for aligning an instruction boundary in variable length macroinstructions with an instruction buffer	712/204
68	US 58190 59 A	☒	Predecode unit adapted for variable byte-length instruction set processors and method of operating the same	712/213
69	US 58190 57 A	☒	Superscalar microprocessor including an instruction alignment unit with limited dispatch to decode units	712/204
70	US 57940 29 A	☒	Architectural support for execution control of prologue and eplogue periods of loops in a VLIW processor	712/241
71	US 57908 21 A	☒	Control bit vector storage for storing control vectors corresponding to instruction operations in a microprocessor	712/200
72	US 57846 03 A	☒	Fast handling of branch delay slots on mispredicted branches	712/234
73	US 57817 89 A	☒	Superscaler microprocessor employing a parallel mask decoder	712/23
74	US 57686 10 A	☒	Lookahead register value generator and a superscalar microprocessor employing same	712/23
75	US 57649 46 A	☒	Superscalar microprocessor employing a way prediction unit to predict the way of an instruction fetch address and to concurrently provide a branch prediction address corresponding to the fetch address	712/239
76	US 57581 16 A	☒	Instruction length decoder for generating output length indicia to identity boundaries between variable length instructions	712/210
77	US 57520 69 A	☒	Superscalar microprocessor employing away prediction structure	712/23
78	US 57485 16 A	☒	Floating point processing unit with forced arithmetic results	708/497
79	US 56995 37 A	☒	Processor microarchitecture for efficient dynamic scheduling and execution of chains of dependent instructions	712/217
80	US 56895 08 A	☒	Reservation ring mechanism for providing fair queued access in a fast packet switch networks	370/391
81	US 56340 26 A	☒	Source identifier for result forwarding	712/217
82	US 56300 83 A	☒	Decoder for decoding multiple instructions in parallel	712/212
83	US 56088 85 A	☒	Method for handling instructions from a branch prior to instruction decoding in a computer which executes variable-length instructions	712/204
84	US 56008 06 A	☒	Method and apparatus for aligning an instruction boundary in variable length macroinstructions with an instruction buffer	712/204
85	US 55901 23 A	☒	Device and method for use of a reservation ring to compute crossbar set-up parameters in an ATM switch	370/397
86	US 55862 77 A	☒	Method for parallel steering of fixed length fields containing a variable length instruction from an instruction buffer to parallel decoders	712/210
87	US 55662 98 A	☒	Method for state recovery during assist and restart in a decoder having an alias mechanism	714/10
88	US 55599 74 A	☒	Decoder having independently loaded micro-alias and macro-alias registers accessible simultaneously by one micro-operation	712/217

	Document ID	U	Title	Current OR
89	US 5537629 A	☒	Decoder for single cycle decoding of single prefixes in variable length instructions	712/210
90	US 5519698 A	☒	Modification to a reservation ring mechanism for controlling contention in a broadband ISDN fast packet switch suitable for use in a local area network	370/411
91	US 5511070 A	☒	Reservation ring mechanism for controlling contention in a broadband ISDN fast packet switch suitable for use in a local area network	370/411
92	US 5471593 A	☒	Computer processor with an efficient means of executing many instructions simultaneously	712/235
93	US 5467347 A	☒	Controlled access ATM switch	370/230
94	US 5386365 A	☒	Rear wheel steering system for vehicle	701/44
95	US 5327420 A	☒	Method for building multi-bit parallel Batcher/banyan networks	370/397
96	US 5325356 A	☒	Method for aggregating ports on an ATM switch for the purpose of trunk grouping	370/397
97	US 5305311 A	☐	Copy network providing multicast capabilities in a broadband ISDN fast packet switch suitable for use in a local area network	370/390

	Document ID	U	Title	Current OR
1	US 20030023835 A1	☐	Method and system to perform a thread switching operation within a multithreaded processor based on dispatch of a quantity of instruction information for a full instruction	712/214
2	US 20030023834 A1	☐	Method and system to insert a flow marker into an instruction stream to indicate a thread switching operation within a multithreaded processor	712/214
3	US 20030023659 A1	☐	Method and apparatus for thread switching within a multithreaded processor	709/102
4	US 20030023658 A1	☐	Method and system to perform a thread switching operation within a multithreaded processor based on detection of the absence of a flow of instruction information for a thread	709/102
5	US 20030018687 A1	☐	Method and system to perform a thread switching operation within a multithreaded processor based on detection of a flow marker within an instruction information	709/102
6	US 20030018686 A1	☐	Method and system to perform a thread switching operation within a multithreaded processor based on detection of a stall condition	709/102
7	US 20030018685 A1	☐	Method and system to perform a thread switching operation within a multithreaded processor based on detection of a branch instruction	709/102
8	US 20020095563 A1	☐	Method and apparatus for using an assist processor to prefetch instructions for a primary processor	712/207
9	US 20020087793 A1	☐	System and method for instruction cache re-ordering	711/125
10	US 20010052064 A1	☐	Value speculation on an assist processor to facilitate prefetching for a primary processor	712/225
11	US 6519683 B2	☐	System and method for instruction cache re-ordering	711/125
12	US 6490658 B1	☐	Data prefetch technique using prefetch cache, micro-TLB, and history file	711/140
13	US 6415356 B1	☐	Method and apparatus for using an assist processor to pre-fetch data values for a primary processor	711/118
14	US 6219780 B1	☐	Circuit arrangement and method of dispatching instructions to multiple execution units	712/215
15	US 6175898 B1	☐	Method for prefetching data using a micro-TLB	711/137
16	US 6018253 A	☐	Register with current-steering input network	326/93
17	US 5978899 A	☐	Apparatus and method for parallel processing and self-timed serial marking of variable length instructions	712/210
18	US 5974534 A	☐	Predecoding and steering mechanism for instructions in a superscalar processor	712/215
19	US 5958041 A	☐	Latency prediction in a pipelined microarchitecture	712/214

	Document ID	U	Title	Current OR
20	US 5898852 A	☐	Load instruction steering in a dual data cache microarchitecture	712/214
21	US 5822555 A	☐	Method and apparatus for aligning an instruction boundary in variable length macroinstructions with an instruction buffer	712/204
22	US 5784603 A	☐	Fast handling of branch delay slots on mispredicted branches	712/234
23	US 5630083 A	☐	Decoder for decoding multiple instructions in parallel	712/212
24	US 5600806 A	☐	Method and apparatus for aligning an instruction boundary in variable length macroinstructions with an instruction buffer	712/204
25	US 5586277 A	☐	Method for parallel steering of fixed length fields containing a variable length instruction from an instruction buffer to parallel decoders	712/210
26	US 5566298 A	☐	Method for state recovery during assist and restart in a decoder having an alias mechanism	714/10
27	US 5559974 A	☐	Decoder having independently loaded micro-alias and macro-alias registers accessible simultaneously by one micro-operation	712/217
28	US 5537629 A	☐	Decoder for single cycle decoding of single prefixes in variable length instructions	712/210
29	US 5535360 A	☐	Digital computer system having an improved direct-mapped cache controller (with flag modification) for a CPU with address pipelining and method therefor	711/140
30	US 5526506 A	☐	Computer system having an improved memory architecture	711/111
31	US 5440707 A	☐	Instruction and data cache with a shared TLB for split accesses and snooping in the same clock cycle	711/3

	Document ID	U	Title	Current OR
1	JP 2003050509 A	☐	RICE TRANSPLANTER EQUIPPED WITH FERTILIZER APPLICATOR	
2	DE 10056655 A1	☐	Instruction based planning system for coordinate or crossbar switch in packet switching system, connects input connection with selective output connections in specific time slot based on reservation status from planning module	
3	EP 744879 A2	☐	Switching system	
4	WO 200273903 A	☐	Bandwidth reservation reuse e.g. for dynamically allocated ring protection and restoration, involves accounting for bandwidth based on source steered restoration with bandwidth reserved on worst case single failure scenario basis	
5	JP 2002079953 A	☐	Lane tracking-control device has arrangement to judge starting reservation condition of steering control, and if it is in control start reservation condition, control start unit makes steering control start	
6	DE 10056655 A	☐	Instruction based planning system for coordinate or crossbar switch in packet switching system, connects input connection with selective output connections in specific time slot based on reservation status from planning module	
7	US 5918034 A	☐	Pipeline stages decoupling method in pipelined microarchitecture	
8	US 5600806 A	☐	Instruction code aligning and rotating method for instruction buffer of processor - involves scanning last byte vector in direction from back to front to locate last byte of last complete instruction within instruction buffer	
9	US 5586277 A	☐	Multiple macro-instruction steering method for instruction decoder - involves supplying first op-code byte vector in which each bit corresponds to one byte in instruction buffer so that each bit indicates whether its associated byte is first non-prefix op-code byte of macro-instruction	
10	EP 744879 A	☐	Switching system having crossbar device for routing data packets in ATM switch - has logic unit with reservation ring in ATM switch which intercepts data exiting from selected evaluator of ring, and processes data to set up switching device for routing data packets	